Claim Amendments

1. (Currently Amended) A packaged integrated circuit device comprising:

a processor;

a volatile memory; ~~and~~

a cross-point memory[[.]];

a substrate including a bus, said processor, volatile memory, and cross-point memory in a vertical stack over said substrate; and

a distinct electrical connection from each of said processor, volatile memory, and cross-point memory to said substrate, said processor, said memories, and said substrate encapsulated within a single package.

2. (Currently Amended) The ~~circuit~~ device of claim 1 including a first die and a second die, wherein said processor is on said first die and said cross-point memory is on said second die.

Claim 3. (Canceled)

4. (Currently Amended) The ~~circuit~~ device of claim 1 also including a phase-change memory.

5. (Currently Amended) The ~~circuit~~ device of claim 1 ~~including a package containing~~wherein said volatile memory and said cross-point memory are stacked over said processor~~dice~~.

Claim 6. (Canceled)

7. (Currently Amended) The ~~circuit~~ device of claim 2 wherein said first die includes a processor and a non-volatile memory.

8. (Currently Amended) The ~~circuit~~ device of claim 1 including a non-volatile memory.

9. (Currently Amended) The ~~circuit~~ device of claim 1 including a ball grid array package.

10. (Currently Amended) A method comprising:

providing a processor and a cross-point memory on separate dice; ~~and~~

providing a substrate including a bus, said separate dice in a vertical stack over said substrate;

electrically coupling each die to said substrate by a separate electrical connection; and

packaging said cross-point memory ~~and~~, said processor, and said substrate in the same package.

11. (Original) The method of claim 10 including packaging a volatile memory on a separate die in said package.

Claim 12. (Canceled)

13. (Original) The method of claim 10 including packaging a phase-change memory in said package.

Claim 14. (Canceled)

15. (Currently Amended) The method of claim 10 including stacking a third die adjacent said die including said memory and over said die including said processor~~said dice on top of one another~~.

16. (Original) The method of claim 10 including packaging a volatile memory in the same package with said processor and said cross-point memory.

17. (Original) The method of claim 10 including providing a ball grid array on said package.

18. (Currently Amended) A packaged integrated circuit comprising:

a first die including a processor; [[and]]

a second die including a cross-point memory; [[.]]

a third die including a memory type other than a cross-point memory; and

a substrate including a bus, each of said first, second, and third die stacked vertically over said substrate and electrically coupled to said substrate by a separate electrical connection.

19. (Currently Amended) The circuit of claim 18 ~~including a~~ wherein said third die ~~with~~ includes a volatile memory.

Claim 20. (Canceled)

21. (Original) The circuit of claim 18 including a phase-change memory.

22. (Currently Amended) The circuit of claim 18 ~~including a plurality of~~ wherein said vertically stacked dice include said second and third die stacked over said first die and adjacent each other.

Claim 23. (Canceled)

24. (Original) The circuit of claim 18 including a ball grid array package.

25. (New) The device of claim 5 wherein said volatile memory and said cross-point memory are positioned adjacent to each other.

26. (New) The device of claim 1 wherein said memories are electrically coupled to said processor through said substrate.